Graphene-Based Logic Circuits: Do We Really Need a Band-Gap?

V. Tenace, A. Calimera, E. Macii, M. Poncino

Politecnico di Torino, Dipartimento di Automatica e Informatica, 10129 Torino, Italy

This work, part of the Graphene@Polito initiative, discusses possible ways to implement graphene-based combinational logic circuits.

It's a matter of facts: silicon-based Complementary Metal Oxide Semiconductor (CMOS) is, today, and will be tomorrow, the reference technology for the industry of mainstream electronic goods. The process is irreversible. At each new technology node, issues that were irrelevant few years before rapidly become a primary source of concerns that require larger and larger efforts to be solved. But whatever the costs of keeping the CMOS up, the cost of not doing that would be far greater. That's true not just for financial reasons (integrated circuits are a result of cumulative investment of hundreds of billions of dollars that big companies do not want to vanish), but also for what concerns the social impact (the growth speed of electronics and the massive production that people are used to see can only be supported by a mature and solid industry). Sustaining CMOS has become an informal contract between the semiconductor industry and its customers to keep technology moving forward at an exponential rate and none has interests in receding it. But there is another important variable of the problem that can't be ignored anymore, namely, the growing demand of applications for wearable and implantable systems for the human body. In this domain of application, instead of the standard figures, like integration density and performance, what really matters are the mechanical properties of the electronic devices: flexibility, stretchability and resilience. This will lead to a new class of electronic applications, e.g., epidermal sensors, eyeball cameras and stretchable LED displays [1]. Within this context, what put graphene on top of other candidates in the race to replace silicon is the fact that it concurrently serves as a flexible substrate and a transport vehicle for electrons. Graphene is flexible, is bendable, is stretchable, but also stronger than iron; in graphene carriers can flow almost at the speed of light, they show high mobility and large temperature stability [2, 3]. Exactly what seems to be a perfect match.

The sad side of the story is that graphene is not a semiconductor. The lack of an energy gap between conduction and valence bands prevents the material to be efficiently turned-off. This works to the disadvantage for digital applications which require a clear separation between logic 0's and 1's. Several solutions have been proposed in the recent years as to overcome this drawback; most of them investigate possible fabrication processes, and/or new alternative composites, that can open a band-gap in the material. In other words, people are looking for possible ways to transform graphene into a semiconductor. For instance, one of the most adopted solution consists of patterning a graphene sheet into narrow stripes, also called graphene nanoribbons (GNRs) [4].

Is this a safe path to reach the goal? Is the band-gap an essential requirement for implementing graphene-based logic circuits? Is this what we need to run some kind of data-processing within graphene? Our position takes distance from what has been proposed so far. We embrace the basic principle that an efficient use of graphene should inevitably exploit its intrinsic properties rather than trying to modify them.

Obviously, the use of pristine graphene into logic circuits implies a departure from the "complementary" design style adopted for semiconductors. Implementing pull-up/down networks made out of devices that can't be completely turned-off would imply excessive static

power and low immunity to noise. We therefore face the problem from an orthogonal direction, that is, identify implementation strategies that can take advantages of the semimetal nature of graphene. The alternative path we propose is a new logic style, referred as the pass-XNOR logic style (PXL hereafter), that can fruitfully exploit the properties made available by electrostatically controlled p-n junctions built on pristine sheets of graphene [5].
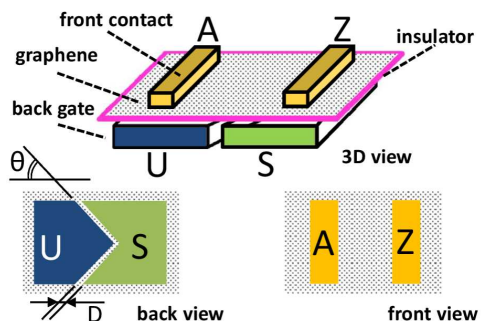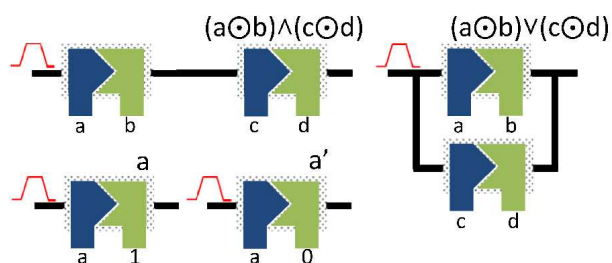

Figure 1. Graphene p-n junction

Figure 2. Simple PXL functions.

A graphene p-n junction, depicted in Figure 1, consists of two back-gates, U and S, which perform the electrostatic doping, and two front metal-to-graphene contacts, A and Z, that work as input and output pins respectively. When U and S are fed with signals having same logic value (both '0'- or '1'-logic), the p-n junction is ON, i.e., it shows a low in-to-out resistive path, connecting Z to A; when U and S have opposite values, the p-n junction turns OFF, i.e., high in-to-out resistive path, isolating Z from A. This resembles the behavior of a transmission gate but with enhanced logic functioning, i.e., the XNOR logic function. The PXL style efficiently integrates such graphene p-n junctions as to implement logical operations on digital signals. PXL can be seen as an extension of a circuitry solution that did not get to success in the semiconductor industry, i.e., Pass-Transistor Logic (PTL). Like PTL, in fact, the information is carried out by means of signal propagation through root-to-sink paths rather than charges stored in parasitic capacitance. Series connections of p-n junctions implement the product between XNOR cubes, parallel connections implement the sum. Complex logic functions are therefore conceived as sum of exclusive-NOR products, as shown in Figure 2. Preliminary simulation results obtained through the use of a Verilog-A [6] model of the p-n junctions show the functionality of circuits implemented with the proposed style, and, most important, their superior in terms of power consumption w.r.t. classical CMOS implementations (1.5-2 orders of magnitude better power efficiency).

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