Double conductance minima in graphene field-effect transistors

A. Di Bartolomeo[1], F. Giubileo[2], F. Romeo[3], R. Citro[3], T. Schroeder[4], G. Lupina[4]*

[1*] Dipartimento di Fisica e Centro Interdipartimentale NANO_MATES, Università di Salerno, Salerno, Italy.
E-mail: dibant@sa.infn.it
[2] CNR-SPIN, Salerno, Italy.
[3] Dipartimento di Fisica, Università di Salerno, Salerno, Italy.
[4] IHP-Microelectronics, Frankfurt (Oder), Germany.

Graphene field-effect transistors (GFETs) have attracted substantial interest for applicability to high-speed electronics and have been extensively used to investigate the electronic transport properties of graphene. In such devices, an electric current is injected/extracted from metallic electrodes (source/drain) through the graphene channel whose conductance is modulated by the electric field from a back- or top-gate. Metal/graphene contacts have been shown to play a significant role in the electrical characteristics of the transistors, and various metals have been employed as electrodes. Transfer characteristics of GFETs, i.e. the drain-to-source current versus gate voltage, I_{DS}–V_{GS}, curves, typically display a symmetric V-shape, with a hole dominated conductance (p-branch) at lower V_{GS} and electron-type transport at more positive gate voltages (n-branch), separated by a valley corresponding to the charge neutrality condition (also known as the Dirac point) with equal electron and hole concentrations. This V-shape reflects the energy distribution of the density of states ($D(E) \propto |E|$), and a conductance dropping to zero at the Dirac point should be expected at low temperature; however, in actual devices, impurities and interaction with the surrounding dielectric introduce local fluctuations in the potential causing a finite density of states at the Dirac point; from the carrier viewpoint, these fluctuations result in localized puddles of electrons and holes which produce an appreciable conductance.
Noticeably asymmetric and/or anomalously distorted p-branches have been reported. The asymmetry between p- and n-branches was initially explained in terms of different cross sections of electron/hole scattering from charge impurities, but more recently the metal/graphene interaction at the contacts has been considered as a key element [1]. It has been found in particular that, even in the case of weak adhesion, as with Au, the metal electrodes cause the Fermi level E_F to shift from the conical point in graphene bands, resulting in doping of graphene either with electrons or with holes. Depending on the polarity of carriers in the bulk of the graphene channel, charge transfer between metal and graphene leads to p–p, n–n or p–n junctions in the vicinity of the contacts which can cause asymmetry.
Nouchi et al [2] have studied transfer characteristics in devices with ferromagnetic metal electrodes, reporting anomalously distorted p-branches, with a sort of additional minimum other than the Dirac point. They explain this effect by considering charge transfer from graphene to metal leads and assuming that the presence of an oxide layer spontaneously formed at the metal/graphene interface suppresses the charge density pinning effect, i.e. favours the modulation of the charge-density of graphene at the metal electrodes by the gate voltage.

References

[1] G. Giovannetti et al., Physics Review Letters 101 (2008) 026803.
[2] R. Nouchi et al., Applied Physics Leters 96 (2010) 253503.
[3] H.-Y. Chiu et al., Nano Letters 10 (2010) 4634–9.
[4] S. Barraza-Lopez et al., Physics Review Letters 104 (2010) 076807.
[5] Y. Nam et al., Carbon 50 (2012) 1987-1999.
[6] T. Feng, et al., Carbon 79 (2014) 363-368.
[7] A. Di Bartolomeo et al., Nanotechnology 22 (2011) 275702.
[8] A. Di Bartolomeo et al., Diamond and Related Materials, 38 (2013) 19-23.

A second conductance minimum to the left of the original Dirac point has also been investigated by H.Y. Chiu et al. [3] for Ti-contacted graphene transistors in the high field regime. They attribute it to a positive charge trapped at the graphene/oxide interface in the vicinity of the drain which would induce the formation of a p–n junction in the drain region. A double dip in the transfer characteristic has been also discussed by Barraza-Lopez et al. [4] with a first-principles study of the conductance through graphene suspended between Al contacts. They show that the charge transfer at the leads and into the freestanding section gives rise to an electron–hole asymmetry in the conductance; more importantly they suggest that, for sufficiently long junctions, this charge transfer induces two conductance minima at the energies of the two Dirac points of the suspended and clamped regions, respectively. Y. Nam and coworkers [5] observed a double dip on graphene structures with both top and bottom gates and attributed it to charge stored in the floating top gate. More recently, T. Feng et al. [6] studied GFET based on chemical vapor deposition grown graphene with double conductance minima that they attribute to the misalignment of the Fermi level between graphene under the metal contacts and in the channel area caused by doping from the contacts.

In this study [7,8] we present measurements on Cr/Au contacted long-channel (~10 μm) graphene transistors on Si/SiO_2 substrate and we report the observation of hysteresis as well as double dips in the transfer characteristics. Charge trapped in the surrounding dielectric and in particular in silanol groups at the SiO_2 surface is at the origin of the hysteresis; while, the gradient of carriers along the channel caused by electron transfer from the graphene to the Au/Cr contacts and the band shift induced by the backgate voltage and the SiO_2-trapped charge are proposed to account for the double dip feature. We show in particular that p–n junctions are spontaneously formed by charge transfer between the graphene and the electrodes and that a double Dirac point can be achieved when low-resistivity contacts are fabricated. We further clarify the role of charge stored at the SiO_2 interface in the formation of the double dip and we propose partial charge pinning at the contacts to explain the current saturation observed at high back-gate voltages. Accordingly, a phenomenological modeling of experimental data is successfully implemented, as shown in Figure 1.

We finally show that the hysteresis, enhanced by a double dip, can conveniently be exploited to build graphene-based memory devices.

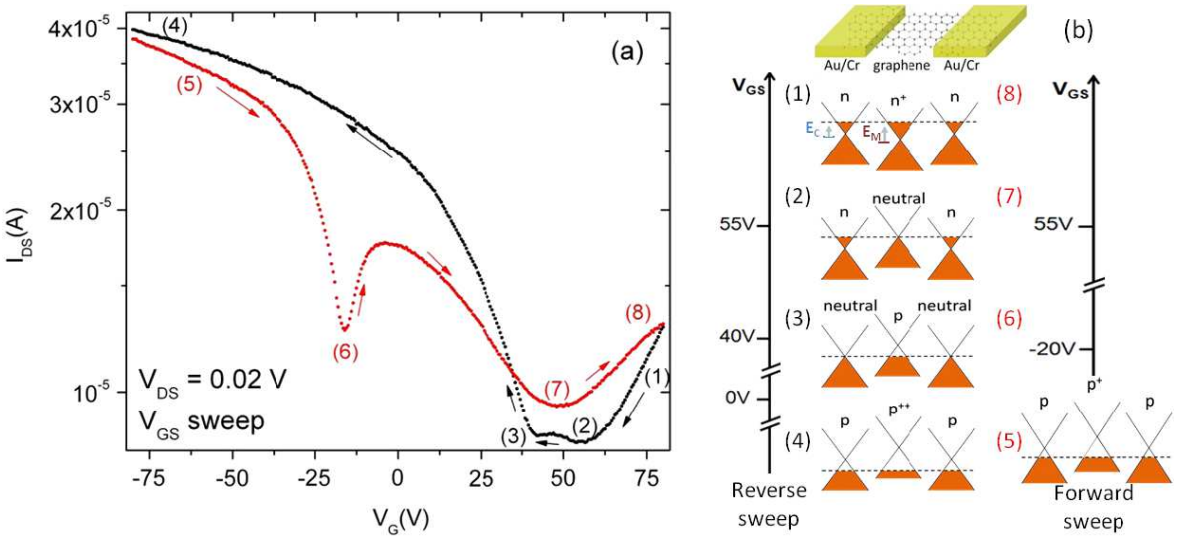

Figure 1: (a) Transfer characteristic of a GFET with hysteresis and a double dip. (b) Band diagrams of the graphene between the source and the drain and position of the Fermi level for different V_{GS}. For a floating gate, the double-cone, close to the contacts, is shifted upward with respect to the one in the bulk channel to account for the p-doping due to transfer of electrons from graphene to the Cr/Au leads.