Ni assisted CMOS Compatible Graphene Synthesis by CVD

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Developments of new approaches for the fabrication of graphene-based microelectronic devices are of the highest importance [1-2]. At this point, appropriate synthesis method, which enables the growth of high quality graphene, is required. However, direct deposition technique, allowing large area, defect-free and uniform graphene layers on arbitrary insulating substrates is still not available (except graphene transfer). In addition, such growth method should be also scalable and compatible with the mainstream Si technology manufacturing requirements. The potential of Ni as a mediator for graphene synthesis has been already investigated by several groups so far, where graphene films were grown via chemical vapor and solid deposition methods at elevated temperatures (~1000 °C) [3-5]. In these cases, graphene growth occurred on top of Ni, underneath Ni and between Ni dots. Although these approaches are very promising, there are also some drawbacks, like the inhomogeneous coverage and number of layers and defects in graphene. In the present work, we show the results of the development of transfer-free, Ni-mediated graphene synthesis method on insulating SiO_2 substrates [6]. This approach benefits from the manufacturing compatibility with Si technologies and avoids the metal contamination problems and complexity associated with graphene transfer from Cu.

In this work, the CVD experiments were performed at the temperatures of 800 – 1000 °C, using C_2H_4 gas as the source of carbon and Ar as a carrier gas. The typical pressures of 0.1 mbar were maintained during the deposition process. Different sets of Ni structures (shown in Fig. 1a-b), were formed on Si wafers, covered with 100 nm thermally grown SiO_2. Carbon content was determined in-situ by X-Ray Photoelectron Spectroscopy, whereas the quality of the deposited carbon was then ex-situ evaluated by Raman spectroscopy.

For the optimization of the growth conditions, experiments of graphene synthesis were initially carried out on top of Ni surfaces. A Raman spectrum of graphene on Ni is shown in Fig. 2, whereas the evolution of Carbon 1 s signal, measured by XPS, is plotted in Fig. 3.Two types of graphene synthesis (underneath and between the Ni structures) routes have been then investigated in this study. The first results of the attempts to grow uniform layers of graphene underneath the Ni structures are presented in Fig. 4. The experiments revealed that the graphene successfully grew underneath the Ni, on the insulating SiO_2 layers, as it was found by Raman spectroscopy, after etching away the top graphene layer and the Ni film. In addition, lateral growth of graphene between Ni structures, directly onto the SiO_2 was also evaluated and presented in Fig. 5. A detailed description of the mentioned graphene synthesis routes and characterization of the layers will be presented.

References

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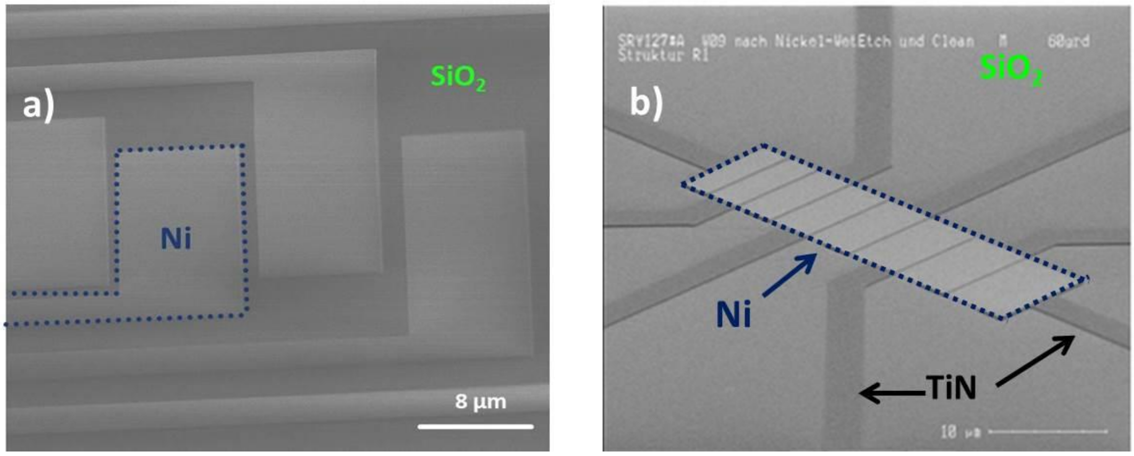

Figure 1: SEM images of different Ni structures on SiO_2/Si wafers.

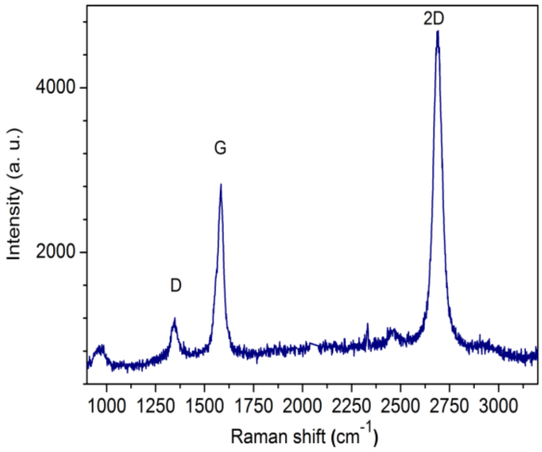

Figure 2: Raman spectra of Graphene on Ni.

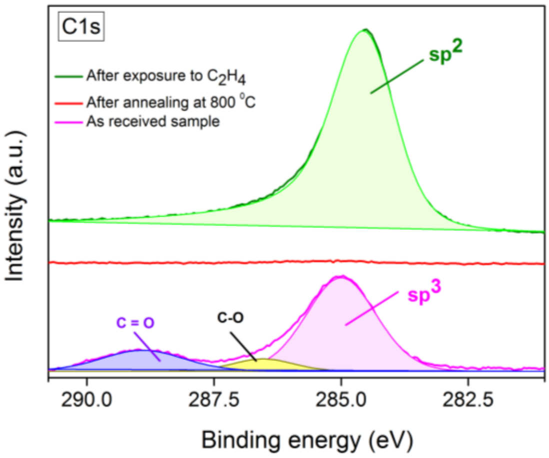

Figure 3: Evolution of Carbon 1s line on Ni/SiO_2 measured by XPS.

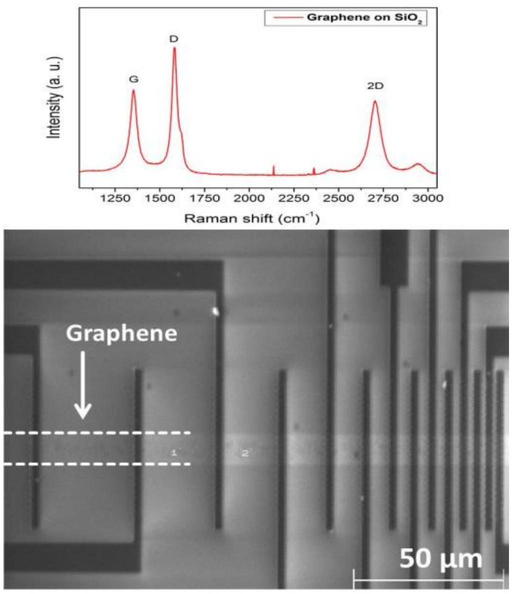

Figure 4: Raman spectra and SEM image of graphene stripe on SiO_2, after the Ni etching.

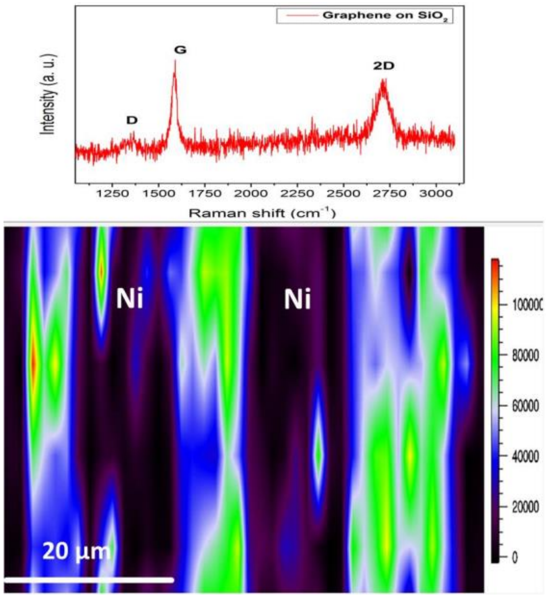

Figure 5: Raman mapping of the 2D intensity of Graphene on SiO_2, grown between Ni Bars.