The Rise of Silicene: from the Synthesis to the Transistor

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Silicene, a honeycomb-like Si lattice, has been so far a fascinating theoretical surmise [1] with no experimental counterpart as due to the natural sp^3 hybridization of Si bonding. Being an atomically thin layer of silicon, silicene attracts an enormous interest as emerging research material for the semiconductor technology roadmap and for its intrinsic affinity with the ubiquitous silicon technology. Free-standing silicene is energetically permitted [1] provided that the chemical bonding are vertically dbuckled rather than being perfectly planar as in graphene. Nonetheless, a stable graphite-like Si allortrope does not exist in nature.

Artificially forcing the silicene lattice was firstly made possible in the epitaxial growth of a Si monolayer on Ag(111) substrates [2]. According to the free-standing silicene model, the epitaxial silicene self-organizes in regularly buckled lattices (namely surface phases) with periodic atomic arrangements as due to the commensurate match with the hosting Ag substrate (see Figure 1(b) as an example of a buckled silicene phase grown on a Ag(111)-based substrate) [3]. Consecutive transitions between silicene surface phases can be observed by tuning the growth temperature in a quite limited window (from 200 to 300°C) and the deposition flux. The buckled arrangement of each silicene phase results in an interplay of sp^2 and sp^3 bonding which causes silicene degradation under environmental conditions according to x-ray photoelectron spectroscopy of the silicene chemical bonding upon ambient exposure. Nonetheless, the hallmark of the silicene lattice can be well-recognized by Raman spectroscopy [4] and the two dimensional (2D) character of the silicene/Ag is shown to bear a characteristic optical response and carrier dynamics. Both these aspects are self-consistently corroborated by *ab initio* modelling.

In view of a subsequent handling of silicene out of the ultra-high vacuum growth conditions, the stability and the interaction with the substrates are the two bottlenecks for the "portability" and the exploitation of silicene in device applications. We here exposed an effective methodology to address both issues and then integrate a silicene layer in a field effect transistor operating at room temperature (see the schematic picture in Figure 1(c)) but prone to degradation in timescale of several minutes [5]. The transfer characteristic of the transistor manifests a graphene-like ambipolar behavior claiming for Dirac fermions as charge carriers although the deduced mobility is comparatively much lower. The silicene transport features are discussed in relation to the structural details of the silicene sheets (coexisting surface phases, point and linear defects, clusters, boundaries, etc.) and to the expected large electron-phonon coupling.

Perspectives to passivate the silicene and then prevent degradation are also envisioned therein including the synthesis of multilayer silicene as well as carefully tailored protective encapsulation approaches. As a future outlook, silicene is also considered as the archetypal X-ene lattice (where X=Si,Ge, Sn,…) which may pave the way to a new class of 2D topological insulators.

References

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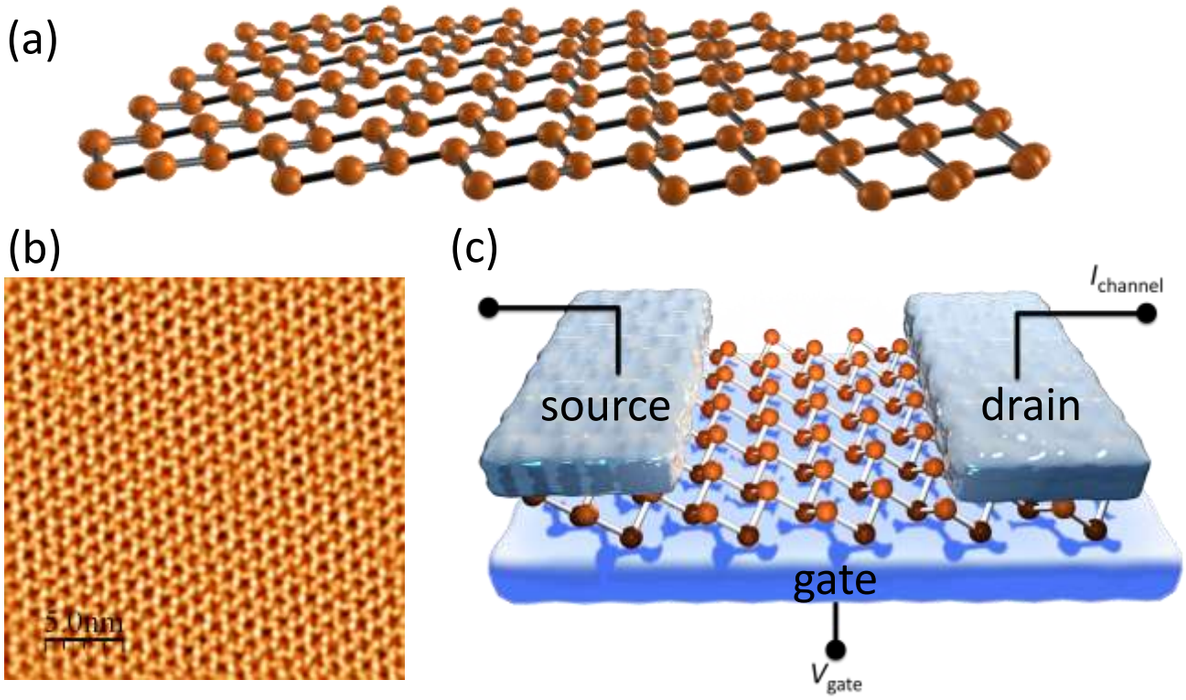

Figure 1 (a) Representative hard sphere model of a free-standing silicene sheet; (b) Scanning tunneling microscopy of a buckled sillicene phase supported by Ag(111); (c) Schematic picture of a silicene-based field effect transistor where the source and drain contacts are made of native Ag and the gate electrode consists of a SiO_2/Si substrate.