OPTIMIZATION OF WAFER-SCALE EPITAXIAL GRAPHENE ON SiC FOR RF APPLICATIONS

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The remarkable electronic properties of graphene [1], especially its high intrinsic mobility [2,3] make it attractive for high speed electronic applications. When annealed at high temperatures, the top layers of SiC undergo thermal decomposition, Si atoms desorb and the carbon atoms remaining on the surface rearrange and re-bond to eventually form epitaxial graphene layers [4-6] (subtractive epitaxy). This process takes place either in vacuum or in an appropriate gas atmosphere [7-12]. Growth of graphene on the Si-face of hexagonal single crystalline SiC (h-SiC) wafers under appropriate conditions exhibits manageable growth kinetics contrary to the case of C-face growth allowing better control over the number of graphene layers. This, coupled with the fact that the azimuthal orientation of epi graphene on the Si-face is determined by the crystal structure of the substrate [4,5], should provide a pathway towards uniform coverage and structural coherence at wafer-scale. These advantages have not been feasible in the case of exfoliated graphene flakes, which otherwise have been invaluable to the study and elucidation of graphene properties and its current popularity, and in polycrystalline graphene CVD films grown on metal catalysts the structural coherence of graphene is also lost at wafer scale [13]. In addition, graphene grown on semi-insulating SiC can be used in situ without having to be transferred to another insulating substrate, as is the case with CVD grown graphene on metals.

However, the Hall mobilities of graphene grown on the Si-face of SiC, as summarized recently [12], are lower than that of graphene flakes, and thus it is important that the graphene growth process is optimized ensuring better performance and property uniformity at wafer scale, to potentially enable practical applications of graphene. Here we are showing results that point towards this goal.

We developed initially a graphene growth process on 4H or 6H (0001) SiC wafers by combining for the first time a cleaning step under a Si-containing gas and an annealing/graphenization at a higher temperature in Argon [12]. SiC was cleaned mainly from oxidic contamination by annealing at 810°C under disilane flow (20% disilane in He). After the cleaning step, the SiC wafer was annealed at 1450°C for 2 min under Ar flow at a pressure of 3.5×10^{-4} Torr. The Hall mobility and field effect mobility in these samples reached up to about 1450 cm^2/Vs at a carrier density n = 2.8e12 cm^{-2} and top-gated radio frequency field effect transistors (RF-FETs) with a peak cutoff frequency fT of 100 GHz for a gate length of 240 nm were fabricated using such epitaxial graphene on SiC (figure 1) [12,14]. In an improved graphene growth process we added an extra annealing step at 1140°C under disilane flow, which results

in a vicinal surface with smooth terraces, as in the example shown in figure 2. Most likely, the surface reconstruction is the C-rich phase $\sqrt{3} \times \sqrt{3}$ [9]. The duration of the graphenization step was increased to 10 min in ∼0.35 mTorr of Ar. The graphenization temperature at this pressure was optimized by a series of runs at different temperatures for 6H(0001) SiC, as shown on figure 3. The optimal graphenization temperature is at 1500°C, with Hall mobilities from large bars (160 μm×200 μm) reaching 1985 cm^2/Vs at carrier density n= 1.24×10^{12} cm^{-2}. Similar optimization has been done for P=3.5 mTorr, where T=1550°C seems to be optimum growth temperature. Figures 4a,b show that our graphene on SiC(0001) has structural coherence and uniform coverage at wafer-scale.

Process optimization would have been impossible if we had not identified the important effect that the SiC wafer miscut angle has on graphene performance. Commercially available "on axis" SiC wafers have a miscut angle specification that varies from 0° to 0.50°. As shown in figure 5, for exactly the same graphene growth process (T=1550°C for 10 min in 3.5 mTorr of Ar), the Hall mobility varies from 586 cm^2/Vs to 1830 cm^2/Vs. This variation is due to the different widths of the vicinal terraces of the graphenized SiC, which is directly linked to the miscut angle. Although the graphenized surface of SiC wafers with high miscut angle (e.g. 0.45°) was pit-free, their mobility was much lower than in wafers with low miscut angle and wider terraces with some pits. It seems that there is a clear correlation between the mean free path of the carriers in graphene (estimated to be a fraction of a micrometer) with the width of the underlying vicinal terraces in SiC.

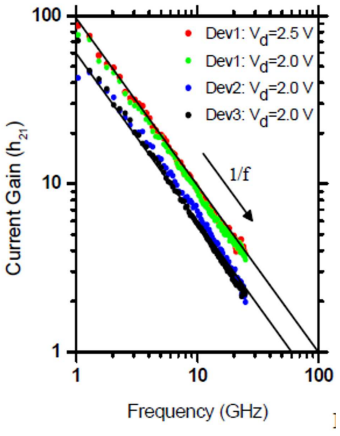

Figure 1: De-embedded current gain $|h_{21}|$ vs. frequency for three RF-FETs (L_G=240 nm) exhibiting a range of cutoff frequencies f_T between 60 and 100 GHz. (data from ref. 12 and 14).

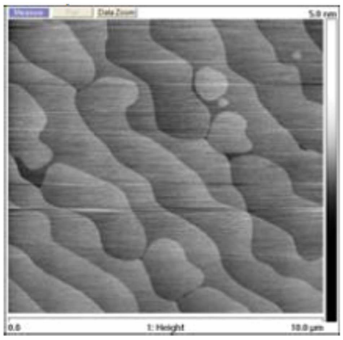

Figure 2: Vicinalized SiC surface after the intermediate 1140°C surface preparation step but before the graphenization step (image is from Cface but shows the effectiveness of this step).

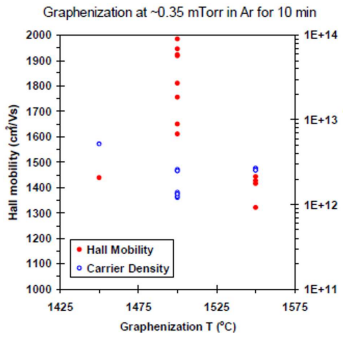

Figure 3: Optimization of mobility vs. temperature at P=0.35 mTorr. Mobility approaches 2000 cm^2/Vs in devices grown at T=1500°C.

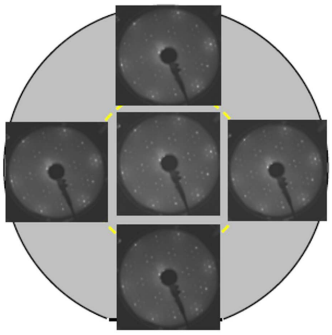

Figure 4: (a) LEED patterns taken at the center of graphenized 2 inch SiC wafer, and on a concentric circle with a 1 inch diameter. The patterns are completely identical.

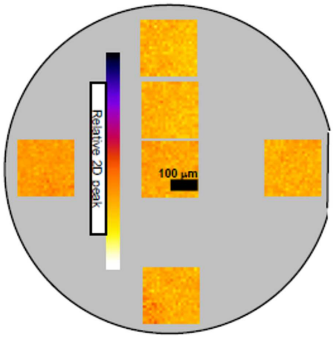

Figure 4: (b) Raman maps depicting the intensity of the 2D peak in various areas of the 2 inch wafer, demonstrating good thickness uniformity of graphene. Each map depicts 200 mm x 200 mm square sampling areas.

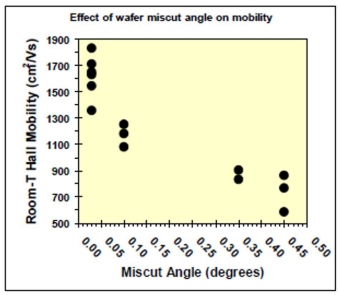

Figure 5: Hall mobility vs. SiC wafer miscut angle.

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