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## HIGH ON-OFF RATIOS IN BILAYER GRAPHENE FIELD EFFECT TRANSISTORS REALIZED BY SURFACE DOPANTS

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For the application of graphene in logic switches transistors with a high on-off ratio are necessary to provide two discrete states. One method to increase the on-off ratio in graphene is the application of a perpendicular field to bilayer graphene. This can be realized with a double gate structure with a bottom and top gate fabricated around the bilayer. In this work we investigate a method to replace one of the gates by surface doping. We fabricated back gated bilayer graphene field effect transistors (GFETs), where the graphene's top side was freely accessible for surface doping. We used highly p-doped Si covered with 90 nm thermally grown SiO<sub>2</sub> as a substrate. Prior to the graphene deposition the substrate was coated with HMDS in a chemical vapor deposition process [1]. A careful preparation of the samples was crucial for the observation of the discussed effects. The graphene was exfoliated with an adhesive tape from a natural graphite crystal and deposited on the substrate. After graphene deposition the contact electrodes were fabricated by optical lithography, sputter deposition of 40 nm nickel and subsequent lift-off. A schematic of the GFET's device stack is depicted in the inset of Fig. 1.

The doping of the upper graphene plane was achieved by two different approaches: The exposure of the device to ambient atmosphere for several hours led to a p-doping of the graphene. Although this method is not suited for device fabrication because of its experimental character, it is rather simple to perform and allows a stepwise removal of the dopants by annealing and therefore a quasi continuous tuning of the doping level. The second approach is based on the evaporation of a 1 nm thin aluminum layer that oxidizes immediately when exposed to ambient atmosphere. Aluminum causes a strong n-type doping in graphene [2]. The sheet resistance  $\rho_{SQ}$  as a function of the applied back gate voltage  $U_{BG}$  of two freshly fabricated bilayer graphene devices with n-type (aluminum) and p-type (atmospheric) doping are depicted in Fig. 1 together with the characteristics of an undoped device at room temperature. We observed that due to the doping not only the charge neutrality point (CNP) of the graphene is shifted to larger values (-42 V for n-type doping and +32 V for p-type doping), but also the resistance at the CNP and the on-off ratio increased. Previous investigations on double-gated bilayer GFETs [3,4] showed a similar behavior and in ARPES studies of doped bilayer graphene the opening of a band gap due to symmetry breaking was observed [5].

For an application oriented evaluation the on-off ratio of a GFET is defined as a figure of merit, governed by the ratio of the resistance at the CNP and the resistance at a carrier concentration of  $10^{13} \text{ cm}^{-2}$ , which corresponds to a back gate voltage of  $\pm 40 \text{ V}$ . In Fig. 2 the on-off ratios  $R_{\text{CNP}}/R_{\text{CNP}\pm 40\text{V}}$  of all investigated devices are plotted as a function of their respective back gate voltage at the CNP. In the n-type regime for negative back gate voltages from -20 to -42 V the on-off ratio reached values between 18 and 43. In the case of atmospheric doping the on-off ratios were between 7 and 40 with the CNP voltages ranging from 10 to 60 V. After annealing at 200 C in nitrogen the GFETs had lost most of their doping as evidenced by the shift of the CNP voltage into the range of -5 to 5 V. As a consequence the on-off ratio was reduced to values between 6 and 10.

The method presented here for increasing the on-off ratio in bilayer graphene by surface doping has the potential to bias a bilayer GFET at an optimal working point and then control the channel by a single gate electrode.

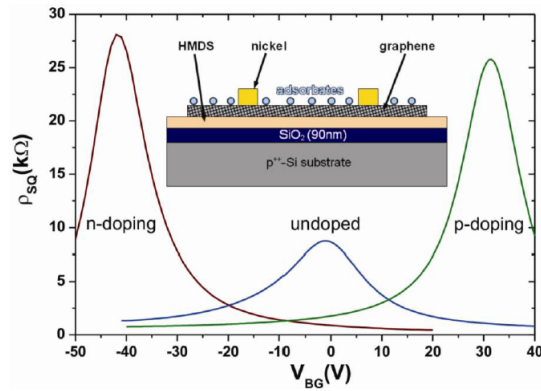


Figure 1: Sheet resistance of n-type, p-type and an undoped bilayer GFET as a function of the applied back gate voltage at room temperature. The inset shows a schematic of the fabricated GFETs. The doping by adsorbates is indicated.

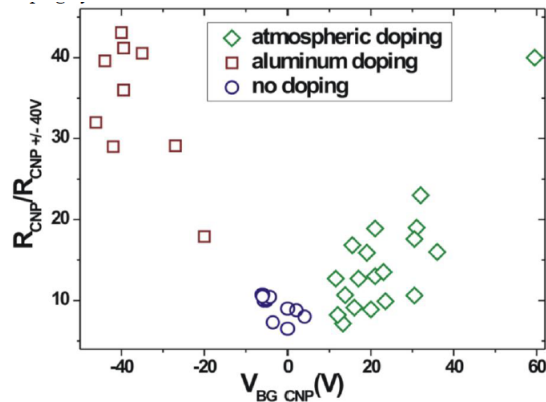


Figure 2: On/off ratio vs. position of charge neutrality point  $V_{\text{BG-CNP}}$  of several devices. All measurements have been performed in nitrogen atmosphere and at room temperature.

**References**

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