GROWTH MECHANISMS OF EPITAXIAL GRAPHENE ON OFF-AXIS 4H-SiC (0001) AND NANO/MICRO-SCALE ELECTRICAL CHARACTERIZATION

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One major challenge towards the development of graphene based electronics is the wafer scale growth of laterally uniform graphene films on substrates compatible with current semiconductor technology. Under this point of view, epitaxial growth of graphene by high temperature induced thermal decomposition of hexagonal SiC represents the most promising method, owing to the fact that graphene is directly obtained on a semiconductor/semiinsulating substrate without any need of transfer. So far, most of the studies on epitaxial graphene (EG) growth have been carried out on on-axis semi-insulating hexagonal SiC. However, in the perspective of future industrial applications, the investigation of the growth process and of the electronic properties of EG on off-axis 4H-SiC (0001) is highly desirable. In fact, such substrates with lowly doped epitaxial layers are the standard platform of current SiC technology and are available as (relatively) low cost large wafers of very high crystalline quality. In this work, we investigated the mechanisms of epitaxial graphene (EG) growth the Si face of 4H-SiC (0001) 8° off-axis, by annealing in inert gas ambient (Ar). A wide temperature range (T_{gr} from 1500°C to 2000°C) was considered. Some of the samples were subjected to an "in situ" hydrogen treatment, with the aim to electrically decouple the grown graphene from the substrate. For each growth temperatures, the number of graphene layers (N_{gr}) was determined locally by high resolution transmission electron microscopy (see Figure 1) and, on several sample positions, by atomic force microscopy (AFM) measuring the depth of selectively etched trenches (by O_2 plasma treatments) in graphene. N_{gr} is found to increase almost linearly as a function of the growth temperature in the considered temperature range (see Figure 2). The few layers of graphene (FLG) are found to cover in conformal way the terraces of the SiC surface. The presence of wrinkles in the FLG films preferentially oriented in the direction perpendicular to the step edges of the SiC terraces is shown.

The electronic properties of the grown layers have been investigated on micrometer scale by standard measurements on test structures (van der Pauw, transmission line model) and locally, on submicrometer scale, by scanning probe methods [1,2]. Top gated field effect transistors were fabricated on EG and electrically characterized (see Figure 3).

PECVD deposited Si_3N_4 was used as a gate dielectric. It showed excellent coverage on EG, without any need of surface functionalization, and minimally affected the conductivity of the film.

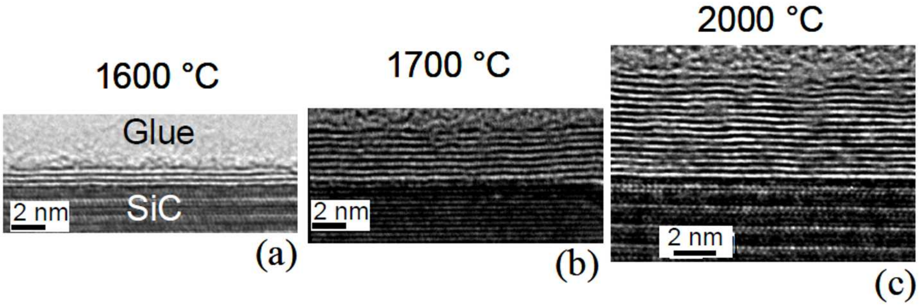

Figure 1: High resolution transmission electron microscopy of graphene layers grown on 4HSiC (0001), 8° off, at different temperatures: 1600°C (a), 1700°C (b) and 2000°C (c).

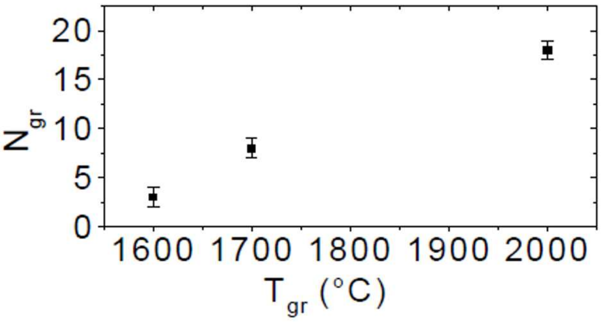

Figure 2: Number of grown graphene layers (N_{gr}) as a function of the growth temperature (T_{gr})

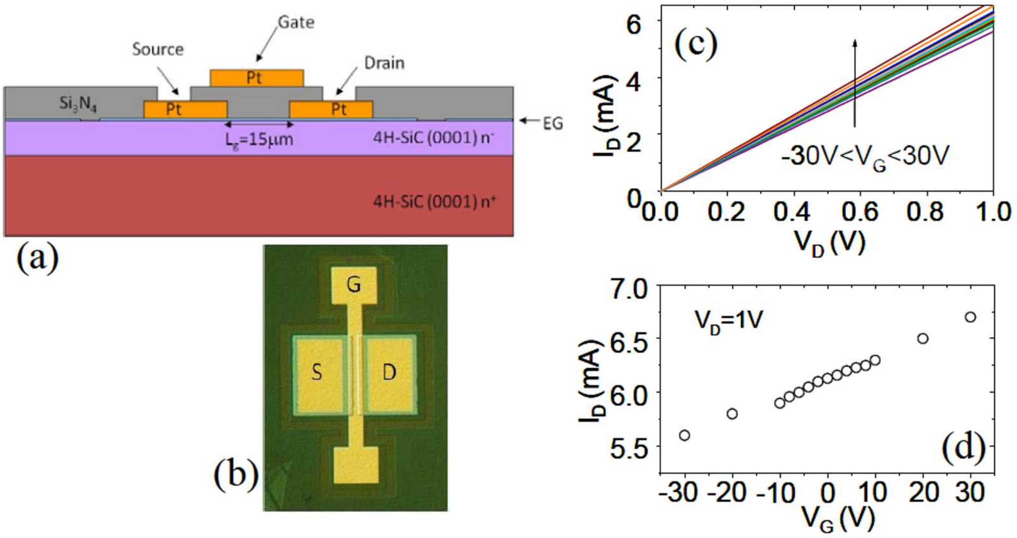

Figure 3: Schematic of the cross section (a) and top view optical image (b) of a field effect device fabricated on epitaxial graphene, using 80 nm Si_3N_4 as gate dielectric. I_D-V_D (c) and I_D-V_G (d) characteristics of the transistor.

References

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